LISTING OF THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously presented) A computer system having a multipath cross bar bus, comprising:

one or more processors;

one or more resources capable of being shared by the one or more processors; and

a resource controller and bus that is connected to each resource and to each processor,

wherein the resource controller is capable of permitting each processor to simultaneously access a different resource from the one or more resources, and

wherein the resource controller includes a hardware semaphore unit for controlling access to the shared resources.

2. (Previously presented) The system of Claim 1, wherein the one or more resources further comprise one or more memory resources and wherein the resource controller further comprises a memory controller that is capable of permitting a first processor to access a first memory resource and a second processor to access a second memory resource at the same time.

3. (Original) The system of Claim 2, wherein the memory controller further comprises one or more switches that are capable of selecting a particular memory resource to connect to a particular processor and a resource arbitration controller that controls the one or more switches in order to dynamically connect each processor independently to each memory resource.

4. (Original) The system of Claim 3, wherein the one or more switches comprise one or more multiplexers.

5. (Original) The system of Claim 4, wherein the resources further comprise one or more peripheral resources and wherein the resource controller further comprises a peripheral controller that is capable of permitting a first processor to access a first peripheral resource and a second processor to access a second peripheral resource at the same time.

6. (Original) The system of Claim 5, wherein the peripheral controller further comprises one or more switches that are capable of selecting a particular peripheral resource to connect to a particular processor and a resource arbitration controller that controls the one or more switches in order to dynamically connect each processor independently to each peripheral resource.

7. (Original) The system of Claim 6, wherein the one or more switches comprise one or more multiplexers.

8. (Original) The system of Claim 1, wherein the resources further comprise one or more peripheral resources and wherein the resource controller further comprises a peripheral controller that is capable of permitting a first processor to access a first peripheral resource and a second processor to access a second peripheral resource at the same time.

9. (Original) The system of Claim 8, wherein the peripheral controller further comprises one or more switches that are capable of selecting a particular peripheral resource to connect to a particular processor and a resource arbitration controller that controls the one or more switches in order to dynamically connect each processor independently to each peripheral resource.

10. (Original) The system of Claim 9, wherein the one or more switches comprise one or more multiplexers.

11. (Previously presented) An apparatus for controlling the access to one or more computing resources by one or more processors, the apparatus comprising a resource controller and bus that is connected to each resource and to each processor wherein the resource controller is capable of permitting each processor to simultaneously access a different resource from the one or more resources, and wherein the resource controller includes a hardware semaphore unit for controlling access to the one or more resources.

12. (Original) The apparatus of Claim 11, wherein the resources further comprise one or more memory resources and wherein the resource controller further comprises a memory controller that is capable of permitting a first processor to access a first memory resource and a second processor to access a second memory resource at the same time.

13. (Original) The apparatus of Claim 12, wherein the memory controller further comprises one or more switches that are capable of selecting a particular memory resource to connect to a particular processor and a resource arbitration controller that controls the one or more switches in order to dynamically connect each processor independently to each memory resource.

14. (Original) The apparatus of Claim 13, wherein the one or more switches comprise one or more multiplexers.

15. (Original) The apparatus of Claim 14, wherein the resources further comprise one or more peripheral resources and wherein the resource controller further comprises a peripheral controller that is capable of permitting a first processor to access a first peripheral resource and a second processor to access a second peripheral resource at the same time.

16. (Original) The apparatus of Claim 15, wherein the peripheral controller further comprises one or more switches that are capable of selecting a particular peripheral resource to connect to a particular processor and a resource arbitration controller that controls the one or more switches in order to dynamically connect each processor independently to each peripheral resource.

17. (Original) The apparatus of Claim 16, wherein the one or more switches comprise one or more multiplexers.

18. (Original) The apparatus of Claim 11, wherein the resources further comprise one or more peripheral resources and wherein the resource controller further comprises a peripheral controller that is capable of permitting a first processor to access a first peripheral resource and a second processor to access a second peripheral resource at the same time.

19. (Original) The apparatus of Claim 18, wherein the peripheral controller further comprises one or more switches that are capable of selecting a particular peripheral resource to connect to a particular processor and a resource arbitration controller that controls the one or more switches in order to dynamically connect each processor independently to each peripheral resource.

20. (Original) The apparatus of Claim 19, wherein the one or more switches comprise one or more multiplexers.

21. (Previously presented) An apparatus for controlling the access to one or more memory resources by one or more processors, the controller comprising a memory resource controller and bus that is connected to each memory resource and to each processor, wherein the resource controller includes a hardware semaphore unit for controlling access to the shared resources, and wherein the memory resource controller is capable of permitting each processor to simultaneously access a different resource from the one or more memory resources.

22. (Previously presented) The apparatus of Claim 21, wherein the memory controller further comprises one or more switches that are capable of selecting a particular memory resource to connect to a particular processor and a resource arbitration controller that controls the one or more switches in order to dynamically connect each processor independently to each memory resource.

23. (Previously presented) The apparatus of Claim 22, wherein the one or more switches comprise one or more multiplexers.

24. (Previously presented) An apparatus for controlling access by one or more processors to one or more peripheral resources, the apparatus comprising a peripheral resource controller and bus that is connected to each peripheral resource and to each processor, wherein the resource controller is capable of permitting each processor to simultaneously access a different peripheral resource from the one or more peripheral resources, wherein the peripheral resource controller includes a hardware semaphore unit for controlling access to the one or more peripheral resources, the hardware semaphore unit being configured to receive requests from the one or more processors and prioritize access based on the requests.

25. (Original) The controller of Claim 24, wherein the peripheral controller further comprises one or more switches that are capable of selecting a particular peripheral resource to connect to a particular processor and a resource arbitration controller that controls the one or more switches in order to dynamically connect each processor independently to each peripheral resource.

26. (Original) The controller of Claim 25, wherein the one or more switches comprise one or more multiplexers.

27. (Previously presented) A computer system, comprising:

a first processor capable of executing a set of instructions;

a second processor capable of executing a set of instructions;

a multipath memory controller having a first bus that is capable of connecting the first processor to a set of memory resources and a second bus that is capable of connecting the second processor to the same set of memory resources wherein the first and second processors are capable of simultaneously accessing different memory resources, wherein the multipath memory controller includes a first semaphore unit for prioritizing access to the set of memory resources; and

a multipath peripheral controller having a first bus that is capable of connecting the first processor to a set of peripheral resources and a second bus that is capable of connecting the second processor to the same set of peripheral resources wherein the first and second processors are capable of simultaneously accessing different peripheral resources, wherein the multipath peripheral controller includes a second semaphore unit for prioritizing access to the set of peripheral resources, wherein

at least one of the semaphore units comprises a hardware semaphore unit.